Microprocessor Supervisory Circuits

ADM690–ADM695

FEATURES

Superior Upgrade for MAX690–MAX695
Specified Over Temperature
Low Power Consumption (5 mW)
Precision Voltage Monitor
Reset Assertion Down to 1 V V_{CC}
Low Switch On-Resistance 1.5 Ω Normal, 20 Ω in Backup
High Current Drive (100 mA)
Watchdog Timer—100 ms, 1.6 s, or Adjustable
600 nA Standby Current
Automatic Battery Backup Power Switching
Extremely Fast Gating of Chip Enable Signals (5 ns)
Voltage Monitor for Power Fail

APPLICATIONS

Microprocessor Systems
Computers
Controllers
Intelligent Instruments
Automotive Systems

GENERAL DESCRIPTION

The ADM690–ADM695 family of supervisory circuits offers complete single chip solutions for power supply monitoring and battery control functions in microprocessor systems. These functions include µP reset, backup battery switchover, watchdog timer, CMOS RAM write protection, and power failure warning. The complete family provides a variety of configurations to satisfy most microprocessor system requirements.

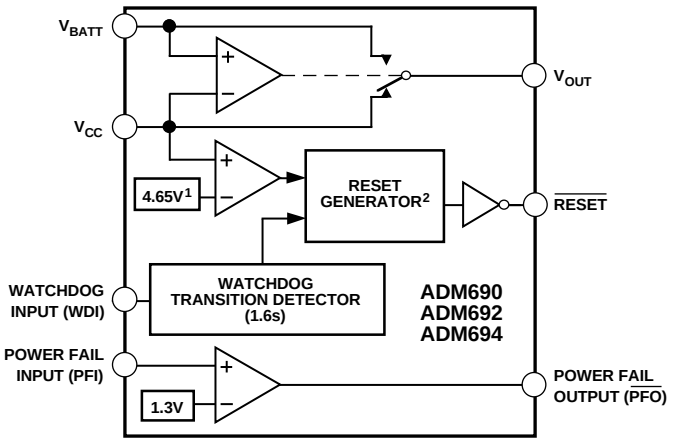
The ADM690, ADM692 and ADM694 are available in 8-pin DIP packages and provide:

1. Power-on reset output during power-up, power-down and brownout conditions. The $\overline{\text{RESET}}$ output remains operational with V_{CC} as low as 1 V.
2. Battery backup switching for CMOS RAM, CMOS microprocessor or other low power logic.
3. A reset pulse if the optional watchdog timer has not been toggled within a specified time.
4. A 1.3 V threshold detector for power fail warning, low battery detection, or to monitor a power supply other than +5 V.

The ADM691, ADM693 and ADM695 are available in 16-pin DIP and small outline packages and provide three additional functions.

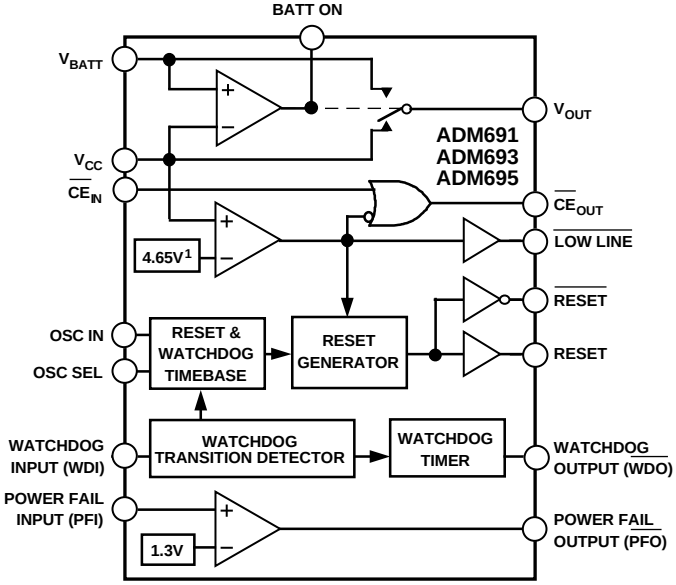
1. Write protection of CMOS RAM or EEPROM.
2. Adjustable reset and watchdog timeout periods.
3. Separate watchdog timeout, backup battery switchover, and low V_{CC} status outputs.

FUNCTIONAL BLOCK DIAGRAMS



[1]VOLTAGE DETECTOR = 4.65V (ADM690, ADM694)
4.40V (ADM692)

[2]RESET PULSE WIDTH = 50ms (ADM690, ADM692)
200ms (ADM694)



[1]VOLTAGE DETECTOR = 4.65V (ADM691, ADM695)
4.40V (ADM693)

The ADM690–ADM695 family is fabricated using an advanced epitaxial CMOS process combining low power consumption (5 mW), extremely fast Chip Enable gating (5 ns) and high reliability. $\overline{\text{RESET}}$ assertion is guaranteed with V_{CC} as low as 1 V. In addition, the power switching circuitry is designed for minimal voltage drop thereby permitting increased output current drive of up to 100 mA without the need for an external pass transistor.

ADM690–ADM695–SPECIFICATIONS

(V_{CC} = Full Operating Range, V_{BATT} = +2.8 V, T_A = T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
BATTERY BACKUP SWITCHING					
V_{CC} Operating Voltage Range					
ADM690, ADM691, ADM694, ADM695	4.75		5.5	V	
ADM692, ADM693	4.5		5.5	V	
V_{BATT} Operating Voltage Range					
ADM690, ADM691, ADM694, ADM695	2.0		4.25	V	
ADM692, ADM693	2.0		4.0	V	
V_{OUT} Output Voltage	V_{CC} – 0.05	V_{CC} – 0.025		V	I_{OUT} = 1 mA
	V_{CC} – 0.5	V_{CC} – 0.25		V	I_{OUT} ≤ 100 mA
V_{OUT} in Battery Backup Mode	V_{BATT} – 0.05	V_{BATT} – 0.02		V	I_{OUT} = 250 µA, V_{CC} < V_{BATT} – 0.2 V
Supply Current (Excludes I_{OUT})		1	1.95	mA	I_{OUT} = 100 mA
Supply Current in Battery Backup Mode		0.6	1	µA	V_{CC} = 0 V, V_{BATT} = 2.8 V
Battery Standby Current					5.5 V > V_{CC} > V_{BATT} + 0.2 V
(+ = Discharge, – = Charge)	–0.1		+0.02	µA	T_A = +25°C
	–1.0		+0.02	µA	
Battery Switchover Threshold		70		mV	Power Up
V_{CC} – V_{BATT}		50		mV	Power Down
Battery Switchover Hysteresis		20		mV	
BATT ON Output Voltage			0.3	V	I_{SINK} = 3.2 mA
BATT ON Output Short Circuit Current		35		mA	BATT ON = V_{OUT} = 4.5 V Sink Current
	0.5	1	25	µA	BATT ON = 0 V Source Current
RESET AND WATCHDOG TIMER					
Reset Voltage Threshold					
ADM690, ADM691, ADM694, ADM695	4.5	4.65	4.73	V	
ADM692, ADM693	4.25	4.4	4.48	V	
Reset Threshold Hysteresis		40		mV	
Reset Timeout Delay					
ADM690, ADM691, ADM692, ADM693	35	50	70	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
ADM694, ADM695	140	200	280	ms	OSC SEL = HIGH, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, Internal Oscillator	1.0	1.6	2.25	s	Long Period, V_{CC} = 5 V, T_A = +25°C
	70	100	140	ms	Short Period, V_{CC} = 5 V, T_A = +25°C
Watchdog Timeout Period, External Clock	3840		4097	Cycles	Long Period
	768		1025	Cycles	Short Period
Minimum WDI Input Pulse Width	50			ns	V_{IL} = 0.4, V_{IH} = 3.5 V
$\overline{RESET}$ Output Voltage @ V_{CC} = +1 V		4	200	mV	I_{SINK} = 10 µA, V_{CC} = 1 V
$\overline{RESET}$, $\overline{LOW\ LINE}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 4.25 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 5 V
$\overline{RESET}$, $\overline{WDO}$ Output Voltage			0.4	V	I_{SINK} = 1.6 mA, V_{CC} = 5 V
	3.5			V	I_{SOURCE} = 1 µA, V_{CC} = 4.25 V
Output Short Circuit Source Current	1	3	25	µA	
Output Short Circuit Sink Current		25		mA	
WDI Input Threshold					V_{CC} = 5 V[1]
Logic Low			0.8	V	
Logic High	3.5			V	
WDI Input Current		20	50	µA	WDI = V_{OUT}, T_A = +25°C
	–50	–15		µA	WDI = 0 V, T_A = +25°C
POWER FAIL DETECTOR					
PFI Input Threshold	1.25	1.3	1.35	V	V_{CC} = +5 V
PFI Input Current	–25	±0.01	+25	nA	
$\overline{PFO}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	3.5			V	I_{SOURCE} = 1 µA
$\overline{PFO}$ Short Circuit Source Current	1	3	25	µA	PFI = Low, $\overline{PFO}$ = 0 V
$\overline{PFO}$ Short Circuit Sink Current		25		mA	PFI = High, $\overline{PFO}$ = V_{OUT}
CHIP ENABLE GATING					
$\overline{CE}_{IN}$ Threshold			0.8	V	V_{IL}
	3.0			V	V_{IH}
$\overline{CE}_{IN}$ Pull-Up Current		3		µA	
$\overline{CE}_{OUT}$ Output Voltage			0.4	V	I_{SINK} = 3.2 mA
	V_{OUT} – 1.5			V	I_{SOURCE} = 3.0 mA
	V_{OUT} – 0.05			V	I_{SOURCE} = 1 µA, V_{CC} = 0 V
$\overline{CE}$ Propagation Delay		5	9	ns	

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
OSCILLATOR					
OSC IN Input Current		±2		µA	
OSC SEL Input Pull-Up Current		5		µA	
OSC IN Frequency Range	0		250	kHz	OSC SEL = 0 V
OSC IN Frequency with External Capacitor		4		kHz	OSC SEL = 0 V, C_{OSC} = 47 pF

NOTE
[1]WDI is a three level input which is internally biased to 38% of V_{CC} and has an input impedance of approximately 125 kΩ.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{CC} . . . . . –0.3 V to +6 V
V_{BATT} . . . . . –0.3 V to +6 V
All Other Inputs . . . . . –0.3 V to V_{OUT} + 0.5 V
Input Current
  V_{CC} . . . . . 200 mA
  V_{BATT} . . . . . 50 mA
  GND . . . . . 20 mA
Digital Output Current . . . . . 20 mA
Power Dissipation, N-8 DIP . . . . . 400 mW
  θ_{JA} Thermal Impedance . . . . . 120°C/W
Power Dissipation, Q-8 DIP . . . . . 500 mW
  θ_{JA} Thermal Impedance . . . . . 125°C/W
Power Dissipation, N-16 DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 135°C/W
Power Dissipation, Q-16 DIP . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 100°C/W
Power Dissipation, R-16 SOIC . . . . . 600 mW
  θ_{JA} Thermal Impedance . . . . . 110°C/W
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
  Extended (S Version) . . . . . –55°C to +125°C
Lead Temperature (Soldering, 10 secs) . . . . . +300°C
  Vapor Phase (60 secs) . . . . . +215°C
  Infrared (15 secs) . . . . . +220°C
Storage Temperature Range . . . . . –65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADM690AN	–40°C to +85°C	N-8
ADM690AQ	–40°C to +85°C	Q-8
ADM690SQ	–55°C to +125°C	Q-8
ADM691AN	–40°C to +85°C	N-16
ADM691AR	–40°C to +85°C	R-16
ADM691AQ	–40°C to +85°C	Q-16
ADM691SQ	–55°C to +125°C	Q-16
ADM692AN	–40°C to +85°C	N-8
ADM692AQ	–40°C to +85°C	Q-8
ADM692SQ	–55°C to +125°C	Q-8
ADM693AN	–40°C to +85°C	N-16
ADM693AR	–40°C to +85°C	R-16
ADM693AQ	–40°C to +85°C	Q-16
ADM693SQ	–55°C to +125°C	Q-16
ADM694AN	–40°C to +85°C	N-8
ADM694AQ	–40°C to +85°C	Q-8
ADM694SQ	–55°C to +125°C	Q-8
ADM695AN	–40°C to +85°C	N-16
ADM695AR	–40°C to +85°C	R-16
ADM695AQ	–40°C to +85°C	Q-16
ADM695SQ	–55°C to +125°C	Q-16

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM690–ADM695 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

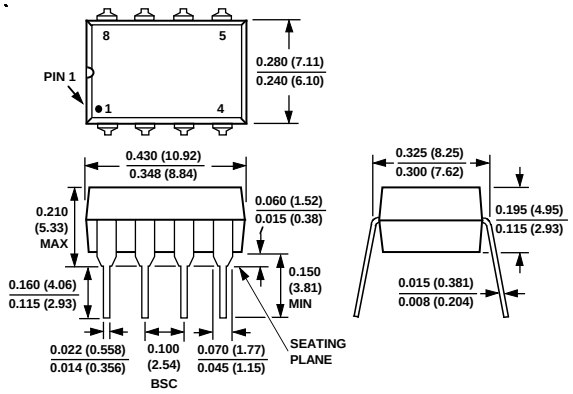
PIN FUNCTION DESCRIPTION

Mnemonic	Function
V_{CC}	Power Supply Input: +5 V Nominal.
V_{BATT}	Backup Battery Input. Connect to Ground if a backup battery is not used.
V_{OUT}	Output Voltage, V_{CC} or V_{BATT} is internally switched to V_{OUT} depending on which is at the highest potential. V_{OUT} can supply up to 100 mA to power CMOS RAM. Connect V_{OUT} to V_{CC} if V_{OUT} and V_{BATT} are not used.
GND	0 V. Ground reference for all signals.
$\overline{\text{RESET}}$	Logic Output. $\overline{\text{RESET}}$ goes low if 1. V_{CC} falls below the Reset Threshold 2. V_{CC} falls below V_{BATT} 3. The watchdog timer is not serviced within its timeout period. The reset threshold is typically 4.65 V for the ADM690/ADM691/ADM694/ADM695 and 4.4 V for the ADM692 and ADM693. $\overline{\text{RESET}}$ remains low for 50 ms (ADM690/ADM691/ADM692/ADM693) or 200 ms (ADM694/ADM695) after V_{CC} returns above the threshold. $\overline{\text{RESET}}$ also goes low for 50 (200) ms if the watchdog timer is enabled but not serviced within its timeout period. The $\overline{\text{RESET}}$ pulse width can be adjusted on the ADM691/ADM693/ADM695 as shown in Table I. The $\overline{\text{RESET}}$ output has an internal 3 μA pull up, and can either connect to an open collector Reset bus or directly drive a CMOS gate without an external pull-up resistor.
WDI	Watchdog Input. WDI is a three level input. If WDI remains either high or low for longer than the watchdog timeout period, $\overline{\text{RESET}}$ pulses low and WDO goes low. The timer resets with each transition on the WDI line. The watchdog timer may be disabled if WDI is left floating or is driven to midsupply.
PFI	Power Fail Input. PFI is the noninverting input to the Power Fail Comparator when PFI is less than 1.3 V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or V_{OUT} when not used.
$\overline{\text{PFO}}$	Power Fail Output. $\overline{\text{PFO}}$ is the output of the Power Fail Comparator. It goes low when PFI is less than 1.3 V. The comparator is turned off and $\overline{\text{PFO}}$ goes low when V_{CC} is below V_{BATT}.
$\overline{\text{CE}}_{IN}$	Logic Input. The input to the $\overline{\text{CE}}$ gating circuit. Connect to GND or V_{OUT} if not used.
$\overline{\text{CE}}_{OUT}$	Logic Output. $\overline{\text{CE}}_{OUT}$ is a gated version of the $\overline{\text{CE}}_{IN}$ signal. $\overline{\text{CE}}_{OUT}$ tracks $\overline{\text{CE}}_{IN}$ when V_{CC} is above the reset threshold. If V_{CC} is below the reset threshold, $\overline{\text{CE}}_{OUT}$ is forced high. See Figures 5 and 6.
BATT ON	Logic Output. BATT ON goes high when V_{OUT} is internally switched to the V_{BATT} input. It goes low when V_{OUT} is internally switched to V_{CC}. The output typically sinks 35 mA and can directly drive the base of an external PNP transistor to increase the output current above the 100 mA rating of V_{OUT}.
$\overline{\text{LOW LINE}}$	Logic Output. $\overline{\text{LOW LINE}}$ goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.
RESET	Logic Output. RESET is an active high output. It is the inverse of $\overline{\text{RESET}}$.
OSC SEL	Logic Oscillator Select Input. When OSC SEL is unconnected (floating) or driven high, the internal oscillator sets the reset active time and watchdog timeout period. When OSC SEL is low, the external oscillator input, OSC IN, is enabled. OSC SEL has a 3 μA internal pull up, (see Table I).
OSC IN	Oscillator Logic Input. With OSC SEL low, OSC IN can be driven by an external clock signal or an external capacitor can be connected between OSC IN and GND. This sets both the reset active pulse timing and the watchdog timeout period (see Table I and Figure 4). With OSC SEL high or floating, the internal oscillator is enabled and the reset active time is fixed at 50 ms typ. (ADM691/ADM693) or 200 ms typ (ADM695). In this mode the OSC IN pin selects between fast (100 ms) and slow (1.6 s) watchdog timeout periods. In both modes, the timeout period immediately after a reset is 1.6 s typical.
$\overline{\text{WDO}}$	Logic Output. The Watchdog Output, $\overline{\text{WDO}}$, goes low if WDI remains either high or low for longer than the watchdog timeout period. $\overline{\text{WDO}}$ is set high by the next transition at WDI. If WDI is unconnected or at midsupply, the watchdog timer is disabled and $\overline{\text{WDO}}$ remains high. $\overline{\text{WDO}}$ also goes high when $\overline{\text{LOW LINE}}$ goes low.

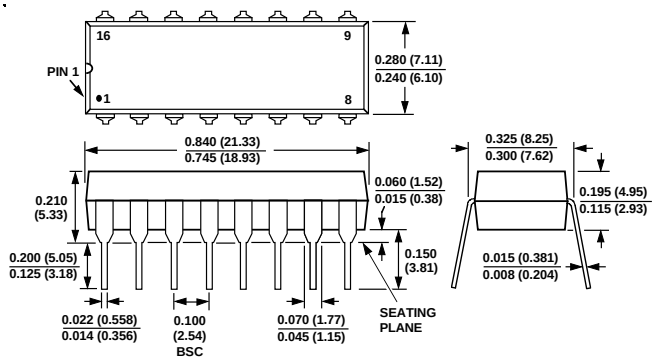
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Pin Plastic DIP (N-8)



16-Lead Plastic DIP (N-16)



8-Pin Cerdip (Q-8)